

**UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION**

SOLAS OLED LTD., an Irish corporation,

Plaintiff,

v.

LG DISPLAY CO., LTD., a Korean corporation; LG ELECTRONICS, INC., a Korean corporation; and SONY CORPORATION, a Japanese corporation,

Defendants.

CASE NO. 6:19-CV-00236-ADA

JURY TRIAL DEMANDED

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

“As the Supreme Court has stated, ‘[i]t seems to us that nothing can be more just or fair, both to the patentee and the public, than that the former should understand, and correctly describe, just what he has invented, and for what he claims a patent.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc) (quoting *Merrill v. Yeomans*, 94 U.S. 568, 573-74 (1876)). Defendants LG Display Co., Ltd., LG Electronics, Inc., and Sony Corporation (collectively, “Defendants”) respectfully ask the Court to apply this fundamental principle of patent law and hold Plaintiff Solas OLED, Ltd. to the words the original patentees used to claim their inventions and to convince the Patent Office to issue the patents-in-suit.

As shown below, Solas turns this core tenet on its ear and refuses to be bound by the unambiguous text of its patents, or even by conventional principles of physics or electrical engineering. It eschews well-established meanings of fundamental terms like “current” and “voltage” and conflates them in an effort to broaden its claims. Similarly, Solas refuses to be bound by conventional uses of the English language. Solas proposes labored meanings of simple words like “before,” “after,” “together,” and “along,” often relying on the trope that some so-called plain and ordinary meaning applies, to try to expand these terms to suit its infringement theories. By contrast, in discerning the meanings of the claim terms, Defendants have looked to the claims, the specifications, and the file histories for guidance as the law requires, and have provided the Court with context in the declaration of Douglas R. Holberg, Ph.D., a seasoned industry veteran, professor, inventor, and author. As a result, Defendants’ proposed constructions “stay[] true to the claim language and most naturally align[] with the patent’s description of the invention,” and so are “in the end, the correct construction[s].” *Phillips*, 415 F.3d at 1316.

II. TECHNOLOGY BACKGROUND

Solas did not invent the technologies described in its patents, which pertain to flat panel

displays. Rather, two of the three patents were awarded to Japanese inventors from Casio who filed them first in Japan in 2004. The third was awarded to a German inventor at the University of Stuttgart who first filed in Germany in 2002. Casio and the University apparently saw no need to hold onto these patents. Solas acquired them, and now asserts them against Defendants' modern-day, organic light-emitting diode displays.

The patents relate to displays in which each pixel has an organic light emitting diode (OLED or OEL). A pixel includes an OLED and a "drive circuit" that is used to control the amount of light emitted by that specific OLED. In such a display, there is an array of (often millions) of such pixels arranged in columns and rows. The "luminance" or intensity of light emitted by each pixel depends on the current driving each OLED. By controlling how much current is supplied to each OLED, the drive circuit can control the level of luminance. The patents in this case pertain generally to how drive circuits for OLEDs work. Below, we discuss several physics and electrical concepts that help inform an understanding of the patents-in-suit and the claims to be construed.

A. Current and Voltage

Current and voltage are distinct but related concepts. Ex. 1¹ (Holberg) ¶¶ 26-29. Current refers to the flow of electric charge.² Voltage refers to the amount of potential energy it takes to move charge between two points.³ Voltage can be used synonymously with "potential," "potential difference," or "electromotive force."⁴ To use a common analogy, one can think of electricity in a circuit like water in a pipe. Current is like the rate at which the water flows, and voltage is like

¹ All citations to "Ex." refer to exhibits to the supporting Declaration of Blake R. Davis.

² Holberg ¶ 26 (citing Ex. 2 (IEEE 100) (2000) at 257; Ex. 3 (Hargrave's Communications Dictionary) (2001) at 131.

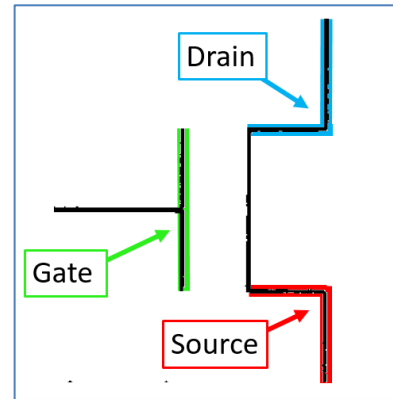
³ *Id.* ¶ 26 (citing Ex. 2 at 1260; Ex. 3 at 572).

⁴ *Id.* ¶ 26 (citing Ex. 2 at 1260 ("voltage is synonymous with potential difference"); Ex. 4 (Microsoft Computer Dictionary) (1997) at 502 ("voltage n. see electromotive force."), 172 ("electromotive force ... also called potential, voltage").

the water pressure that forces the water through the pipe. *Id.* ¶¶ 27-28. While current and voltage are mathematically related, they are distinct phenomena and can be used to serve different functions. *Id.* ¶¶ 29, 32.

B. Thin Film Transistors

Thin film transistors, or TFTs, are key components of OLED drive circuits. A TFT has three electrodes: a “gate,” a “drain,” and a “source;” and a “channel” between the drain and source. The ’068 patent depicts a TFT, as shown here and annotated. ’068 patent at Fig. 2 (cropped, annotated); *see also* Holberg ¶ 30. The gate electrode controls the flow of current through the



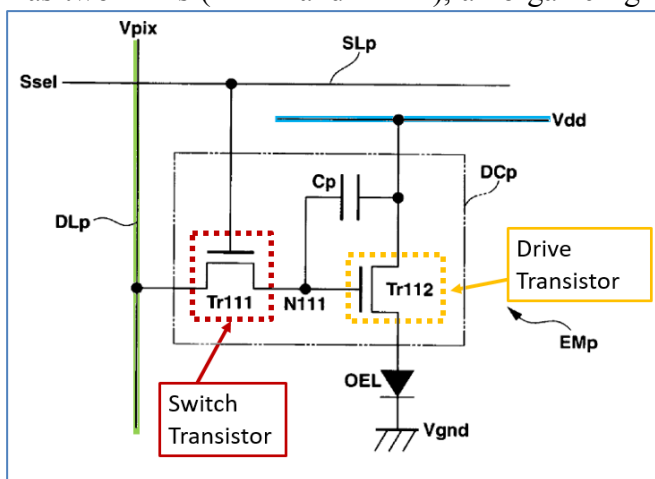
channel. *Id.* ¶ 31. When the **voltage** between the gate and source (the “gate-source voltage” or “gate voltage”) is below a certain “threshold voltage,” no current flows through the channel. *Id.* When the voltage increases above the threshold voltage, the channel becomes conductive (i.e., the transistor “turns on” and the gate is “driven”), allowing current to flow.⁵ Generally, the higher the gate voltage, the greater the current that flows through the channel. Thus, the gate is often referred to as a control electrode, and the drain and source as current-conducting electrodes.

By applying different levels, or gradations, of voltages above the threshold voltage to the gate, a TFT can control the current that flows through it. *Id.* ¶ 33. A TFT also can be used as a switch that either blocks current from flowing or allows it to flow. *Id.* In keeping with the water-in-pipes analogy, applying voltage to the gate of a TFT is like turning a valve on a pipe that can shut the flow of water on or off or control the rate at which the water flows. *Id.*

⁵ *Id.* ¶ 31. The ability of the material from which TFTs are made to conduct electricity in some situations, but not in others, is why they are commonly referred to as “semiconductors.” Silicon is a classic example of a semiconductor. *Id.* ¶ 30.

C. Circuit Diagrams and Symbols

Engineers depict circuits in diagrams using conventional symbols. *Id.* ¶ 34. For example, TFTs are typically shown using the symbol above, and conductive lines through which electricity flows are typically represented by solid lines. *Id.* The patents reflect such conventions in their figures. Figure 36 of the '137 patent, shown here, is an example. In relevant part, it depicts an admitted prior art “display pixel” (EMp) that has two TFTs (Tr111 and Tr112), an organic light emitting diode (OEL), conductive lines between these and other elements (e.g., DLp, Vdd), and other common components like a capacitor (Cp) and a ground potential (Vgnd). '137 patent at Fig. 36 (annotated); *id.* at 1:59-3:5; *see also* Holberg ¶¶ 34-36.



D. Using Voltage to Control Luminance

Voltage can be used to control luminance. Holberg ¶ 37. In the circuit shown above, Tr112 is the driving transistor through which current flows to the OEL, and another transistor Tr111 acts as a switch to control the gate voltage of Tr112. '137 patent, 2:1-10. When Tr111 is turned on, it provides a “gradation **voltage** Vpix” from the “data line (signal line) DLp,” which **voltage** has a “value corresponding to display data” to the gate of the driving transistor. *Id.* at 2:34-41.⁶ The drive transistor allows current to flow from the “supply line” Vdd to illuminate the OEL, according to the value of the voltage at the gate. '137 patent at 2:46-49. “[C]onsequently, the organic EL element OEL operates to emit light with a luminance gradation [i.e., a grade of light emission intensity] corresponding to the display data (the gradation **voltage** Vpix).” *Id.* at 2:49-52.

⁶ All emphasis in quotes has been added unless otherwise indicated.

III. U.S. PATENT NO. 7,907,137

The '137 patent is directed to a current-programmed OLED display. In the claimed drive circuits, “a gradation **current** having a **current** value ... corresponding to display data” flows “via a data line DL toward a drive circuit DC provided on a display pixel PX.” *Id.* at 20:27-53. This contrasts with “conventional” prior art “**voltage** programmed pixels,” which use a **voltage** value to control the luminance of the pixel. *See id.* at 2:64-3:5, Fig. 36 (depicting prior art).

A. “a gradation current having a current value” (claims 10, 36)

Defendants’ Proposed Construction	Plaintiff’s Proposed Construction
An actual current (not voltage) with a value corresponding to a luminance level.	“Gradation current” means “current conveying information about a level.”

Defendants’ construction of this term will make clear to the jury that “a gradation current having a current value” means what it says: an actual current, not a voltage. Solas’s construction, in contrast, would create needless ambiguity. Worse, in rejecting Defendants’ construction, Solas refuses to accept the basic principle of physics that current is “not voltage.” Its reason is obvious: Defendants’ products use voltage-driven drive circuits like the prior art, not current-driven drive circuits. Whatever Solas may mean by its proposed construction, it appears ready to try to improperly read the claimed “gradation current” onto a “voltage” supplied by Defendants’ products.

Claim construction starts with the language of the claim itself, which supports Defendants’ construction. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582, (Fed. Cir. 1996); *Phillips*, 415 F.3d at 1314. The claim term itself uses the word “current” twice, not “voltage,” and requires the “current value” to correspond to a “luminance gradation of the display data.” ’137 patent at 58:5-12, 62:55-64. This contrasts with other limitations using “voltage” for different functions than those performed by the gradation current. For example, claim 10 requires multiple circuits,

some of which generate current (e.g., a gradation signal generation circuit) and others which generate voltage (e.g., a compensation voltage application circuit).⁷ When a patentee uses different terms in this way, it is “presume[d] that those two terms have different meanings.” *SIPCO, LLC v. Emerson Elec. Co.*, 794 F. App’x 946, *3 (Fed. Cir. 2019); *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000).

Next, the specification is often the “single best guide to the meaning of a disputed [claim] term.” *Phillips*, 415 F.3d at 13121. Here, the specification explains that the “drive control operation in the display drive apparatus” includes “writing a **gradation signal** (a **gradation current** having a predetermined current value) corresponding to display data, and allowing the organic EL element OEL to perform a light emitting operation with a desired luminance gradation corresponding to the gradation signal.” ’137 patent at 13:63-67; *see also id.* at 10:51-55. Defendants’ construction expressly reflects this central theme of using a current corresponding to a luminance gradation: “an actual current (not voltage) with a value corresponding to a luminance level.”

The specification further clarifies the difference between a “gradation voltage” and a “gradation current,” recognizing them as different electrical phenomena, not interchangeable synonyms as Solas would have it. For example, the specification teaches that a “gradation voltage” was used in prior art voltage-programmed pixels as a “**voltage value** corresponding to display data ... and applied to the data line” and the OLED “operates to emit light with a luminance gradation corresponding to display data (the **gradation voltage** V_{pix}).” *Id.* at 2:34-41, 2:49-52, 3:6-14, 3:36-41, Fig. 36; *see also id.* at 14:63-67, 15:67-16:5, 20:29-36, 22:4-14, 22:19-24, 22:25-32, 24:2-10,

⁷ *See also, e.g.*, ’137 patent at claims 1-3, 5-22, 24, 27-34, 36-39 (“gradation current,” “current value,” “current control type optical element,” “current path,” “current flow,” “driving current,” “threshold voltage,” “compensation voltage,” “voltage component,” “detecting voltage,” “potential difference,” “supply voltage”).

24:30-37, 28:49-60, 38:10-19, 38:53-58, 56:13-17, Figs. 7, 8, 9 (discussing patent’s use of a “gradation current”). The claims, however, are explicitly limited to a “gradation **current** having a **current value**” to distinguish the claimed inventions from the prior art and its alleged shortcomings. *Id.* at claims 10, 36; *see also id.* at 3:15-41 (shortcomings of voltage gradation). In every embodiment described in the ’137 patent, the drive circuitry supplies a gradation current, not a gradation voltage. *See, e.g., id.* at 21:62-23:14; Holberg ¶¶ 46-49.

Further, “[i]n addition to consulting the specification, we have held that a court ‘should also consider the patent’s prosecution history, if it is in evidence.’” *Phillips*, 415 F.3d at 1317 (citations omitted). The file history eliminates any possible doubt that the applicants limited the claims to providing a current, and not a voltage. Initially, they tried to broadly claim “gradation signals,” without specifying voltage or current. But they were forced to narrow their claims to cover only “a gradation **current** ... as the gradation signal” to overcome prior art.

a gradation signal generation circuit which generates a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of the display data, as a gradation signal corresponding to [[a]] the luminance gradation of the display data, and supplies the gradation signal current to the display pixel through a data line connected to the display pixel;

Ex. 5 at 2. The applicants argued that a prior art reference, Ono (Ex. 6), did not anticipate the claims because it “discloses **applying a voltage** by addition of a data voltage V_d and the threshold voltage V_{th} to the data line 7,” and therefore “Ono et al **does not disclose** generating and supplying **a gradation current** as a gradation signal.”⁸ Ex. 7 at 32 This unequivocal disavowal of claim

⁸ This distinction between gradation voltage drive circuits and gradation current drive circuits was well known in the art. Holberg ¶¶ 52-53 (describing prior art references).

scope supports construing “gradation current” to make clear that it is “not a voltage.”

Solas’s construction finds no such support in the intrinsic record. To the extent Solas may try to use it to allege infringement by a voltage signal, that should be foreclosed now in claim construction. And, while the intrinsic record consistently describes the claimed “gradation current” as having a value that corresponds to a *luminance gradation* specifically, Solas would improperly broaden the term to “convey” arbitrary “information” about any undefined “level.”

Finally, in meeting and conferring with Defendants, Solas argued that construing this term in part as “not voltage” is improper for using a “negative construction.” Not so. Constructions making clear what is not included in a claim, to head off future disputes, are wholly appropriate. *See, e.g., Trs. of Columbia Univ. in N.Y. v. Symantec Corp.*, 811 F.3d 1359, 1367-68 (Fed. Cir. 2016) (construing term to have negative “attack-free” limitation where “nothing in the specification describes any embodiment which uses attack data to build the model”); *RFID Tracker, Ltd. v. Wal-Mart Stores, Inc.*, 342 F. App’x 628, 630 (Fed. Cir. 2009) (statements in specification and prosecution history supported construction limiting term to “not a transmitter”); *Cave Consulting Grp., LLC v. OptumInsight, Inc.*, 725 F. App’x 988, 994 (Fed. Cir. 2018) (negative limitation supported by specification which limited method to one technique “as opposed to another used in prior art methods”); *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1376-79 (Fed. Cir. 2008) (affirming construction with negative limitation excluding features in disclaimed prior art); *Mangosoft Intellectual Prop. v. Skype Techs. SA*, No. 2:06-CV-390, 2008 U.S. Dist. LEXIS 62281, at *25 (E.D. Tex. Aug. 14, 2008) (“The court concludes that the term ‘migrate’ does not encompass replication or copying. Rather, it requires a change of the location of a directory part.”).

B. “gradation signal” (claims 10, 15, 36, 37, 39)

Defendants’ Proposed Construction	Plaintiff’s Proposed Construction
A gradation current with a current value sent to a pixel to set a luminance gradation	Signal conveying information about a level

This claim term is closely tied to “gradation current,” discussed above, with the added requirement that the gradation current is being used as a “signal.” Defendants’ construction applies the proper meaning of “gradation current,” while making clear that that current serves as a “signal” because it is sent to a pixel to set a luminance gradation. This construction comes straight from the unambiguous claim language—*see* ’137 patent at claims 10 and 36 (the “gradation current” is “supplie[d] ... *to the display pixel*,” and “allow[s] the optical element to perform a light emitting operation *at a luminance corresponding to a luminance gradation* of the display data.”)—and comports with the specification and file history for the same reasons discussed above with respect to the gradation current. *Supra* at Section III.A; *see also* ’137 patent at 10:52-55, 13:63-67, 15:67-16:5, 24:2-17, 24:22-48, 28:49-60, 38:10-19. Solas, by contrast, ignores the claim language that makes clear that only the “gradation current having a current value” is “generated ... *as a gradation signal*,” ’137 patent at claims 10 and 36, and improperly seeks to broaden the claims such that the “gradation signal” could be any “signal” conveying information about any “level.” This is unsupported by the record and should be rejected for the reasons set forth above.

C. “generates, as the gradation signal, a non-light emitting display voltage having a predetermined voltage value” / “a non-light emitting display voltage having a predetermined voltage value for allowing the optical element to perform a non-light emitting operation is generated as the gradation signal” (claims 15, 39)

Defendants’ Proposed Construction	Plaintiff’s Proposed Construction
Indefinite.	Not indefinite.

The dispute here rises and falls with the construction of “gradation signal.” When “gradation signal” in independent claims 10 and 36 is correctly construed as a “gradation current” (and

not voltage), it becomes clear that claims 15 and 39—which would apply a voltage as “the gradation signal” of independent claims 10 and 36—makes no sense and cannot be reasonably understood by a person of ordinary skill in the art. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 898–99 (2014).

This incongruity in the claims comes from the amendment discussed above, in which the applicants abandoned their effort to claim any “signal” of any type, and narrowed the claims to cover only a gradation current as the gradation signal. *Supra* at Section III.A. What the applicants apparently forgot to do, however, is ensure that this amendment carried over to any dependent claims referring back to the generic “gradation signal” they originally claimed. More specifically, dependent claims 15 and 39 refer back to “*the* gradation signal” recited in the independent claims⁹ (which was amended to mean a *current*), but then purport to narrow them to cover only a “*voltage*” as the gradation signal. While this narrowing limitation in the dependent claims may have made sense when the original independent claims still recited a gradation signal of any kind, it cannot be harmonized with the amended claims which require only a current gradation signal. In sum, because the applicants chose to limit “gradation signal” to mean *current* and not voltage, the dependent claims continuing to refer to voltage are nonsensical and indefinite. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357 (Fed. Cir. 1999) (holding where “claims are susceptible to only one reasonable interpretation and that interpretation results in a nonsensical construction of the claim as a whole, the claim must be invalidated”).

⁹ The “antecedent basis” rule compels that the dependent claims’ use of “*the* gradation signal” must refer back to “*a* gradation signal” in the independent claims. Indeed, these terms would lack a proper antecedent basis and be indefinite unless construed in this manner. *See Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249 (Fed. Cir. 2008) (explaining a claim could be indefinite “if a term does not have proper antecedent basis where such basis is not otherwise present by implication or the meaning is not readily ascertainable”).

**D. “through a data line ... through the data line ... through the data line”
(claims 10, 36)**

Defendants’ Proposed Construction	Plaintiff’s Proposed Construction
The gradation current is supplied, the threshold voltage is detected, and the compensation voltage is applied through the same data line.	Plain and ordinary meaning. “A data line” means “one or more data lines.” The antecedent basis for “the data line” is “a data line.”

Claims 10 and 36 of the ’137 patent recite the following:

- “supplies the gradation current to the display pixel through a data line” / “supplying . . . a gradation current having a current value . . . as a gradation signal to the display pixel through the data line”;
- “detects a threshold voltage peculiar to the drive element of the display pixel through the data line” / “detecting a threshold voltage peculiar to the drive element through a data line”; and
- “applies the compensation voltage to the drive element through the data line” / “applying the compensation voltage to the drive element through the data line.”

Both sides agree that the claims require all of these functions (supplying, detecting, and applying) to be performed through “a data line.” And both sides agree that references to “the data line” in the later limitations (the “detecting” and “applying” limitations in claim 10, for example) refer back to the same “a data line” recited in the first limitation (the “supplying” limitation in claim 10). Defendants apply settled case law to interpret the claims to require that, as a result, all of the claimed functions must be performed by the *same* data line, but Solas would ignore that law and expand the claim to permit those functions to be performed by different data lines.

The antecedent basis (“*a* data line” in the supplying limitation) for “the data line” in the detecting and applying limitations, supports that all three functions are performed by the same “*a* data line,” and Solas does not dispute this. Instead, Solas attempts to cloud the issue by misapplying the unremarkable patent law principle that the word “a” can mean “one or more.” Solas urges this construction so it later can argue that one line or set of multiple lines can perform one subset of the required functions, and a different line or lines can perform the remainder, and that

this will somehow equate to “the data line” in the claims. This argument should be rejected.

The Federal Circuit considered this issue in *In re Varma* and rejected the same type of misplaced reliance on the word “a.” 816 F.3d 1352 (Fed. Cir. 2016). At issue was whether a requirement that “*a* statistical analysis request corresponding to two or more selected investments” could be interpreted as multiple statistical analysis requests. *Id.* at 1363-64. The court concluded that the use of “a” did not negate the singular meaning required by the claim language: “For a dog owner to have ‘a dog that rolls over and fetches sticks,’ it does not suffice that he have two dogs, each able to perform just one of the tasks.” *Id.*; *see also Tico, Inc. v. EchoStar Commc’ns Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008) (construing “assembl[ing] said video and audio components into an MPEG stream” to require a single MPEG stream).¹⁰ As the claims clearly refer to the same, singular data line in referring to the different functions it provides, Solas’s attempt to split the functions to “one or more” different data lines should be rejected. Indeed, the applicants disclaimed such an approach during prosecution. The applicants added “through the data line” to the claims and argued that, because Ono (discussed *supra* at Section III.A) disclosed the supplying and applying steps on one line and detecting on a second line, Ono did not disclose detecting “through the data line” as amended. Ex. 5 at 2; Ex. 7 at 32.

E. “before” (claim 10) and “after” (claim 36)

Term	Defendants’ Proposed Construction	Plaintiff’s Proposed Construction
“before”	Earlier in time (not at the same time).	Plain and ordinary meaning.
“after”	Later in time (not at the same time).	Plain and ordinary meaning.

¹⁰ *See also Plano Encryption Techs., LLC v. Alkami, Inc.*, No. 2:16-CV-1032-JRG, 2017 WL 3654122, at *10 (E.D. Tex. Aug. 23, 2017) (“Here, however, each claim recites a particular medium and then recites limitations as to instructions that are stored on the medium and that are to be executed by a processor. Thus, one particular medium must store all of these instructions.”); *LBS Innovations, LLC v. BP Am. Inc.*, No. 2:12-CV-00407-JRG, 2014 WL 61050, at *2 (E.D. Tex. Jan. 7, 2014) (claim to “a data field” required a single data field “containing all the information necessary to be considered ‘a data field’”).

Claim 10 requires “appl[ying] the compensation voltage to the drive element through the data line *before* the gradation signal generation circuit supplies the gradation current to the display pixel.” Claim 36 recites the same requirement in reverse, stating that the gradation current is provided “*after*” the compensation voltage is applied. This clear claim language,¹¹ the specification, and prosecution history, make clear that the compensation voltage must be applied earlier in time than the gradation current—they cannot be applied at the same time.

The specification shows the compensation voltage being applied earlier than a gradation current without any overlap in time. In particular, the compensation voltage (“PRE-CHARGE VOLTAGE V_{pre} ”) is applied during a precharge period that entirely precedes the writing period during which the gradation current (“GRADATION CURRENT I_{data} ”) is applied. *See* ’137 patent at Fig. 7; *id.* at 18:58-19:20, 21:62-22:14, 38:35-40 (“pre-charge voltage” is applied “immediately before the writing operation of the display data”), 47:40-44 (same).

The prosecution history is conclusive on this point. In response to a double patenting rejection, the applicants explained that “before” means that the “voltage corresponding to the threshold voltage” must have been “*previously applied*” before the drive element “is supplied with the gradation current.” Ex. 7 at 28. The applicant contrasted this with the claims of another patent, wherein a “compensated gradation voltage” was generated “by adding a gradation voltage to a compensation voltage,” which meant that the “compensation voltage and the gradation voltage are added to be supplied [*sic*: supplied] at the same time as a compensated gradation voltage.” *Id.* at

¹¹ Defendants’ constructions of “before” and “after” are consistent with the plain and ordinary meaning of these terms. *See, e.g.*, Ex. 8 (American Heritage Dictionary) (2000) at 161-62 (“after” : “*Subsequent* in time to; at a later time than”; “before” : “Previous to in time; earlier than”); Ex. 9 (Bloomsbury English Dictionary) (2004) at 162 (“after” : “later in time than”; “before” : “earlier than a date, time or event”); Ex. 10 (Random House Webster’s Dictionary) (2001) at 63-64 (“after” : “later in time than”; “before” : “previous to; earlier than”).

29 (emphasis original). And the applicant concluded that applying these signals “at the same time” “does not render obvious” supplying a “gradation current ... after application of a compensated voltage.” *Id.* (emphasis original). The applicants then made this point *again* in distinguishing the Ono reference discussed in Section III.A above, arguing that because Ono discloses “applying a voltage obtained by *addition* of a data voltage V_D and a threshold voltage V_{th} ” it “does not disclose applying a compensation voltage *before* supplying a gradation current.” *Id.* at 32. The Court should adopt Defendants’ construction and prevent Solas from arguing that the “plain and ordinary meaning” of “before” and “after” includes the simultaneity it discredited in the prior art.

IV. U.S. PATENT NO. 7,432,891

The ’891 patent addresses a well-known problem where manufacturing differences across the drive transistors can affect the amount of current provided to each OLED, causing different amounts of light to be emitted at the same voltage. ’891 patent, 1:14-21, 1:22-36 (discussing “driver current fluctuations”). To solve this problem, the ’891 patent adds a third TFT to the basic two-TFT drive circuit, discussed *supra* at Sections II.C, II.D, so that the “diode driving current” is tapped, supplied to a current measuring circuit, and, depending on that measured current, a correcting voltage is provided to the data conductor. ’891 patent at 2:11-17. The third transistor thus provides a “current feedback” so that after it is switched off, the current through the OLED is stabilized. *Id.* at 2:17-18, 3:8 (“for current feedback, the circuit has a third film transistor T3”).

A. “current measuring” (claims 1, 3)

Defendants’ Proposed Construction	Solas’s Proposed Construction
Measuring actual current (not voltage).	Plain and ordinary meaning.

“Current measuring” should be construed to mean what it says: measuring actual current, not voltage. Solas apparently wants to argue (as it is doing in parallel proceedings in Germany),

that “current measuring” is expansive and includes measuring voltage. Given this very real dispute, Solas’s proposal that some undefined “plain and ordinary meaning” applies is legally deficient. *O2 Micro Int’l Ltd. v. Beyond Innov. Tech. Co.*, 521 F.3d 1351, 1362–63 (Fed. Cir. 2008).

The claims repeatedly and expressly refer to current being driven, conducted, tapped, and measured (e.g., “a current-driving transistor,” “a current-conducting electrode,” “a driving conductor taps a diode driving current,” “a current measuring and voltage regulating circuit,” “a current measuring result”). ’891 patent at claims 1, 3. As in the ’137 patent, the claims also recite voltage and distinguish it from current and recite it as performing different functions (e.g., “... voltage regulating circuit,” “providing to the data conductor a voltage signal,” “a voltage comparison”). *Id.* Given this different usage, “current measuring” does not mean “voltage measuring,” and Solas’s arguments to the contrary should be put to rest. *CAE Screenplates*, 224 F.3d at 1317.

The specification describes the invention exclusively as using a “**current measuring** and voltage regulating” circuit that produces a “measured value **of the current**,” but never as a voltage-measuring circuit or one that produces a measured value of any voltage. ’891 patent at 2:11-16 (“With this circuit, the current to be measured ...”); *see also, e.g. id.* at 2:3-7 (“dependent on current measurement results”), 2:37-41 (“current measuring”), 3:16-21 (“Depending on the measured current ...”), 3:28-31 (“current measuring circuit”). Indeed, the specification uses “voltage” twenty eight (28) different times yet never once mentions measuring voltage. ’891 patent at Abstract, 1:19, 1:35, 1:37, 1:38, 2:3-7, 2:10, 2:39, 3:6, 3:12, 3:18-19, 3:22, 3:26, 3:29.

The prosecution history solidifies that “current measuring” cannot be construed to include measuring voltage. To secure their patent, the inventors argued that a prior art “Hunter patent is disclosing a **potential** [*i.e.*, voltage] (or a potential difference) measurement, but **clearly not a current measurement**” like the claimed invention. Ex. 11 at 5. Solas then argued to the Patent Office

correctly that there is a “*fundamental difference between voltage and current [that] is known to anyone.*” *Id.* at 4-5. By “clearly characterizing the invention” as being limited to measuring current in its arguments to “overcome rejections based on prior art,” the inventors distinguished and disclaimed measuring voltage from the claims. *Computer Docking*, 519 F.3d at 1374; *Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258, 1274 (Fed. Cir. 2001) (finding arguments that prior art is “‘completely different’ from the invention’s system” supported limiting scope of term “mode” to only the modes disclosed in the claim).

Because (1) the ’891 patent “repeatedly describes the invention” as measuring current, (2) the patent “never identifies the invention” as measuring voltage, and (3) “the sum of the [Solas’s] statements during prosecution would lead a competitor to believe that [Solas] had disavowed coverage of” measuring voltage, Solas should be held to those disclosures and not permitted to recapture now, in litigation, the same voltage measuring it surrendered. *Computer Docking*, 519 F.3d at 1379. Accordingly, “current measuring” should be construed to mean “measuring an actual current (not voltage).”

B. “a third thin film transistor which during driving its gate ...” (claims 1, 3)

Defendants’ Proposed Construction	Solas’s Proposed Construction
The claimed “providing” by the current measuring- and voltage regulating circuit (“said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison”) <i>is</i> required to occur during driving of the third thin film transistor’s gate.	Plain and ordinary meaning. The claimed “providing” by the current measuring- and voltage regulating circuit (“said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison”) <i>is not</i> required to occur during driving of the third thin film transistor’s gate.

The parties’ dispute over this limitation is not one requiring redefinition of the words that are used, but the Court’s ruling on the scope of the claim and whether a series of functions must all happen, as the claims expressly state, “during driving” of the gate of a third film transistor, or

whether one function in that series—the “providing” function—is somehow exempt from this clear claim language as Solas would have it. The dispute is best understood by viewing the claim as a whole. The limitation at issue begins, “a third thin film transistor which *during driving its gate* ...” and goes on to recite three functions: (1) tapping, (2) supplying, and (3) providing:

1. A driving circuit for an image point of an image screen which has an organic light-emitting diode, comprising a capacitor; a feedback coupling; a first thin film transistor as a current-driving transistor for the diode; a second transistor which is connected by a current-conducting electrode with a gate of said first transistor and by a second current-conducting electrode with a data conductor and by its gate electrode with a scanning signal conductor; a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison so that the diode driving of said gate of said third transistor due to its linear switching characteristic acts as a switch for a current deviation in said current measuring- and voltage regulating circuit.

The parties do not dispute that the tapping and supplying functions occur during the driving the gate. The only question is whether the third “providing” function does as well.

Once again, the claim language answers this question, as the grammatical structure and syntax supports only Defendants’ construction. *Credle v. Bond*, 25 F.3d 1566, 1571 (Fed. Cir. 1994). Representative claim 1 above contains a preamble (“A driving circuit ...”) and five limitations: (a) “a capacitor”; (b) “a feedback coupling”; (c) “a first thin film transistor”; (d) “a second transistor”; and (e) “a third thin film transistor which during driving its gate” The inventors used semicolons (annotated with red boxes in the claim above), to demarcate these “separate and distinct” limitations. *In re Affinity Labs of Texas, LLC*, 856 F.3d 902, 907 (Fed. Cir. 2017) (finding

limitations “offset by semicolons” to “strongly indicate[] that each step is separate and distinct”), *cert. denied sub nom. Affinity Labs of Texas, LLC v. Iancu*, 138 S. Ct. 1692 (2018); *3Com Corp. v. D-Link Sys., Inc.*, 473 F. Supp. 2d 1001, 1012 (N.D. Cal. 2007). If the inventor had intended the third providing function *not* to happen “during driving” of the third thin film transistor’s gate, then he would have and could have separated it with a semicolon to stand apart as a sixth, discrete limitation. He did not. And the absence of any punctuation separating this clause “suggests that a single limitation prefaced by [a third transistor which during driving its gate]” was intended. *3Com*, 473 F. Supp. 2d at 1012.

Later in the claim language, the inventors emphasize again that the result of the “providing” function—that there is “a current deviation in said current measuring and voltage regulating circuit”—also happens “*during driving*” of the gate:

a third thin film transistor *which during driving its gate ... providing* to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison, *so that* the diode *during driving of said gate* of said third transistor due to its non-linear switching characteristic acts as a switch for a current deviation in said current measuring- and voltage regulating circuit.

’891 patent at claim 1; *see also id.* at 1:64-2:10, 2:11-18. The only natural reading of this limitation is that the providing function, like the tapping and supplying functions of the limitation, happens “during driving” the gate of the third transistor. *See Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 975 (Fed. Cir. 2017) (“the most natural reading of the limitation is one that incorporates all the steps from the beginning of the attempt to access the telephone network to the end of that attempt.”). Furthermore, and as Dr. Holberg explains, the patent’s only figure confirms to a person of ordinary skill in the art that the “providing” function occurs during driving the gate. Holberg ¶¶ 60-61 (analyzing Figure 1), ¶¶ 57-59; *see also* ’891 patent at 3:9-21 (disclosing that the “third thin film transistor” is used for “current feedback”), claims 1, 3 (“a feedback coupling”).

For these reasons, the “third thin film transistor” limitation should be constrained by the

words the applicant used to claim it including the twice-repeated requirement that its functions be performed “during driving” its gate, and not construed to read the “providing” function out of the limitation as Solas urges.

C. “wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode” (claim 3)

Defendants’ Proposed Construction	Solas’s Proposed Construction
Wherein all above mentioned elements of the driving circuit are electrically connected to the anode or cathode of said light emitting diode.	Wherein all above mentioned elements of the driving circuit are electrically connected to and physically located on the same side of the layers of said light emitting diode.

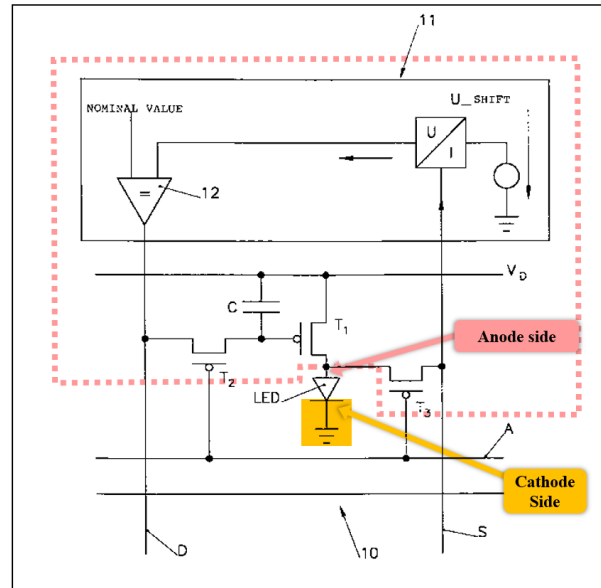
Both sides agree that “wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode” in claim 3 requires the driving circuit elements to be electrically located at, i.e., electrically connected to, the same side of the OLED. The dispute is whether the claim requires those elements also to be “physically located” on the same side as well. The intrinsic record demonstrates that it does not.

The “light emitting diode” in the ’891 patent, like any diode, has an electrode on each of its two sides. ’891 patent at Fig. 1; Holberg ¶ 63. Specifically, the patent’s circuit has “an organic, light-emitting diode LED with a *cathode* connected to ground[]” (’891 patent at 2:64-65), and its “circuit parts” connected entirely to the other “*anode*” side. *Id.* at 2:25-27; *see also* Ex. 12 (“Bu”), [5] (“[A]ll OLEDs” include “one or more layers of organic material,” called an Organic Electro-Luminescent layer (OEL), “sandwiched between *two electrodes*,” i.e., an anode and a cathode) (cited by ’891 patent at 1:32-36¹²); Holberg ¶¶ 63-67. The specification always refers to the relevant elements in the context of their connection to the anode or the cathode and never illustrates or describes the layers of materials that make up the elements as being, or needing to be, physically

¹² Prior art references that are cited by an issued patent are intrinsic evidence for construction of that patent. *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005).

located in any particular orientation to the OLED. '891 patent at Fig. 1, 2:26-2:28. A “side” of the diode thus is either the anode or cathode in the circuit diagram, not any physical layers.

The file history eliminates any doubt that the “same side of the light emitting diode” refers to the electrical connections being on either the cathode or anode side of the diode, consistent with Defendants’ construction. The applicant explained that this requirement is “*clearly shown in the drawings.*” Ex. 13 at 4. The '891 patent has a single drawing, right, a circuit diagram using common engineering



symbols. Holberg ¶¶ 67-68. This circuit diagram depicts no actual shape, form, or geometry of a physical circuit, much less any “layers” of the OLED as Solas argues. Rather, the diagram shows only that the drive circuit elements are electrically located and connected to the anode side of the diode. *Id.*

Solas’s construction does not provide the jury with any helpful explanation of the words used in the claims. Instead, Solas adds new and unsupported words, changing “located” to “*physically* located” and “the same side of said light emitting diode” to “the same side of *the layers* of said light emitting diode,” a practice the Federal Circuit has “repeatedly rejected.” *Source Vagabond Sys. Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1299 (Fed. Cir. 2014) (rejecting construction that “added language without support from the specification or prosecution history”).

V. U.S. PATENT NO. 7,573,068

According to the '068 patent, a problem arises if supply lines are formed in the same layer as a TFT’s electrodes (gate, source and drain). '068 patent at 1:57-2:12. If patterned in the same

layer, the supply lines are thin like the TFT electrodes, which increases the resistance of the supply line, hindering the flow of current to the pixels (like water moving through a narrowed pipe). *Id.* at 2:5-14. The '068 patent purports to solve this problem by forming “feed interconnections” in a separate layer and stacking them on the supply lines. *Id.* at 3:60-4:14. Because the feed interconnections are formed in a different layer than the TFT electrodes, they can be thicker, and thus have lower resistance, suppressing the problems caused by supply lines in the thin TFT layers. *Id.*

A. “formed on said plurality of supply lines along said plurality of supply lines” (claim 1) / “connected to said plurality of supply lines along said plurality of supply lines” (claim 13)

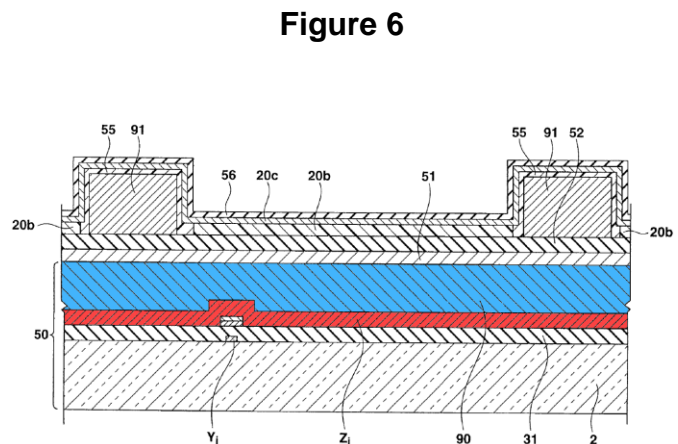
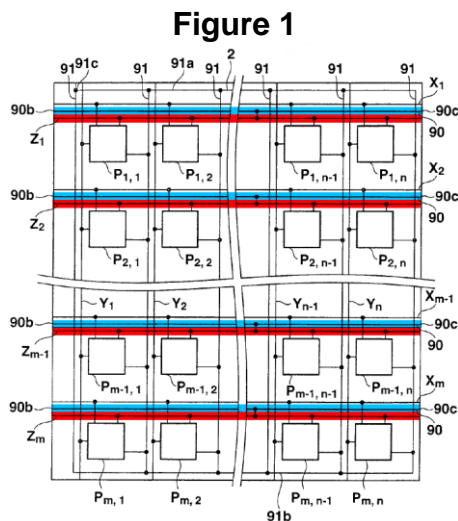
Defendants’ Proposed Construction	Solas’s Proposed Construction
Formed on said plurality of supply lines over the length of said plurality of supply lines.	Formed on said plurality of supply lines over the length or direction of said plurality of supply lines.
Connected to said plurality of supply lines over the length of said plurality of supply lines.	Connected to said plurality of supply lines over the length or direction of said plurality of supply lines.

The dispute centers around the term “along,” which describes how the claimed “feed interconnections” are “formed on” or “connected to” the plurality of “supply lines.” The Court should construe “along” to mean “over the length of” the supply lines, which is how the inventors use the term in the specification. Solas would add the words “or direction” to Defendants’ construction—but from its infringement contentions and the extrinsic evidence it cites, Solas appears poised to try to use its construction to argue that “along said plurality of supply lines” can be satisfied if the feed interconnections merely intersect with the supply lines at any one point, even at oblique or orthogonal angles. This construction finds no support in the intrinsic record.

The claim language requires that the feed interconnections be formed on or connected to the supply lines over a length of the supply lines, not that they merely intersect at a point or points. Just like a series of houses built “along” a first road would be built over the length of that road,

and not at a single point or on a second road that happens to intersect with the first road, the feed interconnects here must do the same. This use of the term “along” in the claims is nothing more than the conventional, customary meaning of the word in English. *See, e.g.*, Ex. 14 (The American Heritage College Dictionary (2002)) at 39 (“1. **Over the length of**: walked along the path.”); Ex. 15 (Webster’s New World College Dictionary (2002)) at 40 (“1. On or beside the length of; **over and throughout the length of** [we hiked along the trail; along the driveway there is a hedge].”); Ex. 16 (Collins English Dictionary Complete and Unabridged (2003)) at 45 (“1. **Over or for the length of**, esp in a more or less horizontal plane: along the road.”); Holberg ¶¶ 73-87.

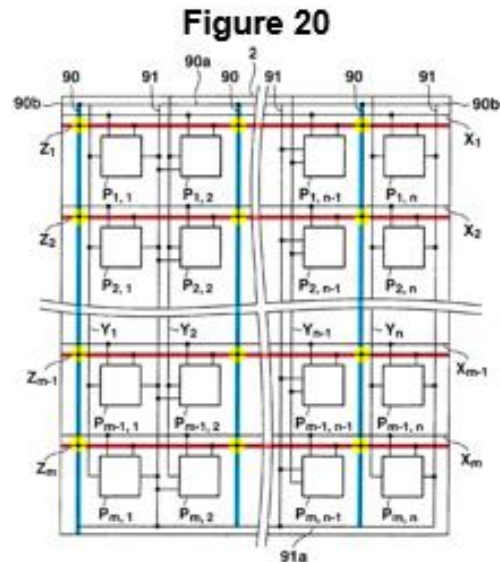
The specification, the “single best guide” to determining the meaning of this claim term, *Phillips*, 415 F.3d at 1321, discloses two embodiments of “feed interconnections,” both of which are formed on or connected to the supply lines **over the length** of the supply lines. The first embodiment is shown below in annotated Figures 1 and 6:



The “feed interconnects” (blue) “are provided in parallel to and on the supply lines” (red). ’068 patent at 6:2-4. Thus, each “feed interconnection” extends over a length of a “supply line” in the horizontal direction. The side view in Figure 6 likewise shows a feed interconnection (blue) formed on and over a length of a supply line (red). ’068 patent at 10:17-29.

In the second embodiment, shown in Figure 20, “[t]he feed interconnections” (blue) “are connected to the supply lines” (red) in a grid. *Id.* at 23:1-3. Every feed interconnection is connected to every supply line, so there are numerous connections—shown in yellow—along the red supply lines. *Id.* at 27:6-11, Figs. 20, 25. Again, these connections are over a length of the supply lines like a series of houses built along streets.

The purpose of having feed interconnections positioned along the supply lines—and not just at a single point—is to reduce resistance. ’068 patent at 2:5-14, 3:61-4:14. As the specification explains, the “feed interconnections are *stacked on* the supply lines” and *formed separately* from the drains, sources, and gates of the driving transistor so that they can be thicker than the thin TFT layers. *Id.* at 3:61-4:14. This increased thickness of the



“stacked” supply lines and feed interconnections reduces the resistance of current flowing to a pixel, minimizing voltage drops and signal delays. *Id.*; see also *id.* at 10:25-32, 18:26-40, 26:62-66; Holberg ¶¶ 81-88. Thus, feed interconnections either get formed on or connect to supply lines over the length of the supply lines. ’068 patent at Figs. 1, 6, 20, 25; see *id.* at 20:25-33. This makes sense; in order to reduce the resistance of current flowing to any pixels, the feed interconnections must contact the supply lines along the lengths that connects the pixels, not at some arbitrary point or points. *Id.* at 6:26-35, 20:24-33, 23:13-21; Holberg ¶¶ 85-88.

Solas adds “or direction” to Defendants’ construction. On its face, this seems minor. However, what Solas intends to argue is that its construction encompasses “feed interconnections” formed or connected at *a single point* “along” the supply lines, rather than “over their length or

direction.” This is reflected in Solas’s selective reliance on a present-day Internet definition of “along” to mean “in a line matching the length or direction of walking along the road also: *at a point or points on* a house along the river.” Ex. 17 (Solas’s Disclosure of Extrinsic Evidence) at 9. This interpretation is also reflected in Solas’s infringement contentions, wherein the structures alleged to be “feed interconnections” are connected to the “supply lines” at only a single point at the edge of the display screen. Ex. 18 at 14-15.

Solas’s interpretation must be rejected. There is not a single disclosure in the specification of a feed interconnection connected or formed on a supply line only at a point—rather, every description confirms the feed interconnections are placed over the length of the supply lines. Thus, Defendant’s construction more naturally aligns with the specification, and should be adopted. *Phillips*, 415 F.3d at 1316.

B. “patterned together” (claims 1 and 13)

Term	Defendants’ Proposed Construction	Solas’s Proposed Construction
“Patterned”	Formed in a single layer.	Formed in one or more layers.
“Patterned together”	Patterned at the same time.	Patterned to fit together.

Independent claims 1 and 13 include the same two “patterned together” requirements: (1) “a plurality of signal lines which are *patterned together* with the gates of said plurality of driving transistors” and (2) “a plurality of supply lines which are *patterned together* with the sources and drains of said plurality of driving transistors.” The disputes are whether “patterned together” encompasses structures that are formed in different layers and at different times. Solas argues that it does, but is wrong for two reasons. First, the well understood meaning of “patterned,” as shown in the specification, refers to forming components in a single layer. Second, the specification makes clear that “patterned together” means patterned at the same time.

The ’068 patent uses the term “patterned” in the context of “manufacturing the display

panel,” which is an integrated circuit comprising transistors, capacitors, organic light emitting diodes, and conductive lines. ’068 patent at 1:15-20, 1:63-2:4, 14:17-15:40. “Patterned” describes how different layers are formed one by one to form the components and lines of the display panel using three well-known semiconductor manufacturing steps: “deposition,” “photolithography,” and “etching.” *See, e.g., id.* at 14:22-27, 14:42-50; *see also id.* at 14:32-34 (“Vapor deposition, photolithography, and etching are sequentially executed to pattern[.]”), 14:34-37 (same), 14:38-41 (same); 15:1-6 (same); *see also id.* at Figs. 5, 6, 7, 8, 9, 10, 24, 25 (showing that components described as “patterned” in the specification are formed in single layers); Holberg ¶¶ 93, 103-114.

As explained in a 2002 textbook by Dr. Holberg, these well-established process steps are used to create “all integrated circuits.”¹³ Ex. 19 at 23-24. By depositing a layer, subjecting it to photolithography, and etching it, the layer is “patterned.” *Id.*; Holberg ¶¶ 94-102. As the textbook explains, and as the specification of the ’068 patent confirms, “this process must be repeated for *each layer* of the integrated circuit.” Ex. 19 at 24; ’068 patent at 14:17-15:40 (describing layer by layer manufacturing), Figs. 5-11, 22-25; Holberg ¶¶ 103-114.

The specification is conclusive that “patterned” refers to forming a single layer or film. The specification discloses that the signal lines and gates and capacitor electrodes “are formed, using photolithography and etching, by *patterning a single conductive film.*” ’068 patent at 9:18-28; *see also id.* at 9:2-4 (“The drains 21d to 23d and source 21s to 23s of the transistors 21 or [sic] 23 are formed by *patterning the same material layer.*”), 9:36-51 (“the drains 23d and sources 23s of the driving transistors 23 ... and the supply lines Z₁ to Z_m are formed, using photolithography

¹³ (1) “Deposition” refers to the step of depositing a layer of material across the surface of a substrate; (2) “photolithography” refers to the step of creating a “mask” for transferring a desired pattern to the layer; and (3) “etching” refers to removing only the portions of the deposited layer that are unprotected by the mask. Ex. 19 at 23-24; Holberg ¶¶ 94-102.

and etching, by *patterning a single conductive film.*”), 25:4-10.

The specification also confirms that the conventional understanding of “patterned together” was patterned at the same time or simultaneously.¹⁴ In conventional OLED TFT arrays, “interconnections such as a power supply line ... are *patterened simultaneously*” with a TFT electrode. *Id.* at 1:57-62. Put differently, “a conductive thin film” is deposited and then “subjected to photolithography and etching to form the [TFT] electrode” and “[a]t the same time, an interconnection [such as a supply line] is also formed.” *Id.* at 1:63-2:1. The “gates” of the TFTs and the “signal lines ... are *simultaneously formed*, using photolithography and etching, *by patterning* a conductive film.” *Id.* at 25:4-10; *see also, e.g., id.* at 11:11-14, 26:40-43 (describing “conductive lines 51 are patterned together with the pixel electrodes 20a by etching a conductive film”), Fig. 8 (showing conductive lines 51 and pixel electrodes 20a in the same patterned layer).¹⁵

Nowhere does the specification ever use the word “patterned” to describe forming more than one layer, or to form the elements of the claims that are “patterned together” at different times. Similarly, Solas’s addition of the words “to fit” so that the term “patterned together” would read “patterned to fit together,” finds no support in the intrinsic evidence. The words “to fit” and even the concept of “fitting” appear nowhere in the claims, specification, or the prosecution history, and so Solas’s construction “violates nearly every tenet of claim construction and amounts to a wholesale rewriting of the claim” that must be rejected. *Source Vagabond*, 753 F.3d at 1301.

¹⁴ “Patterned together” meaning “patterned at the same time” is also supported by the textbook understanding above, which describes photolithography and etching occurring in a single step across an entire deposited layer of material. *See Holberg* ¶ 102.

¹⁵ Defendants’ construction is also supported by additional intrinsic evidence: the prior art cited on the face of the patent. For instance, prior art U.S. Patent No. 7,317,429 discloses that when a film is patterned to form various circuit elements—e.g., gates, sources and drains, scan lines, current lines—the patterning is performed in the “*same step*.” ’429 patent at 7:64-8:13.

“Patterned” thus should be construed as “formed in a single layer,” and “patterned together” as “patterned at the same time.” “Where, as here, a patent repeatedly and consistently characterizes a claim term in a particular way, it is proper to construe the claim term in accordance with that characterization.” *Wis. Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018) (internal quotes and citations omitted) (finding a narrower construction of “prediction” warranted based on the specification’s consistent characterization of the term).

C. “signal lines” (claims 1 and 13)

Defendants’ Proposed Construction	Solas’s Proposed Construction
Conductive lines supplying a value corresponding to a luminance level.	Conductive lines supplying signals.

The parties agree that the “lines” in this claim term are “conductive lines.” But, rather than simply repeating that “signal” means “signal,” as Solas does, Defendants’ construction clarifies that the claimed “signal lines” carry a specific type of signal in the context of this patent: a value corresponding to a luminance level. Solas proposes no construction for “signal,” likely so it can later argue that *any* conductive line in a circuit carrying *any* signal can satisfy this limitation. The claim language and specification support only Defendants’ construction.

The claims recite three different “lines,” each of which carries electrical signals of some sort: signal lines, supply lines, and scan lines. *See, e.g.*, ’068 patent at claim 1 (“a plurality of *supply lines* ... which are arrayed to cross said plurality of *signal lines*”), claim 2 (“[a] substrate according to claim 1, further comprising a plurality of *scan lines* patterned together with the sources and drains ...”). This establishes that “signal lines” has a different meaning than “supply lines” and “scan lines. *CAE Screenplates*, 224 F.3d at 1317. The specification provides decisive guidance on exactly what these different lines are and what types of signals they carry.

The ’068 patent defines and distinguishes “signal lines” from the other two types of conductive lines. In “conventional” OLED panels, “scan lines, signal lines, and power supply lines”

are used in conjunction with “driving transistor[s]” and “switching transistor[s]” that are “arranged for each pixel” to display an image. ’068 patent at 1:21-36; *see also id.* at Figs. 2 and 21, 7:4-26, 24:42-63. The “**supply line**” supplies the driving current that flows through the drive transistor to illuminate the OLED. *Id.* at 1:30-36, 1:41-46. The “**signal line**” supplies the “image data” that is “applied to the gate of the [drive] transistor,” wherein the “image data” is a “**level representing the luminance**” of the OLED. *Id.* at 1:34-36; *see also id.* at 19:17-19, 25:10-12 (“signal lines Y1 to Yn are interconnections to which a . . . **value corresponding to the display gray level flows.**”). The “**scan line**” turns on or off the switching transistor that controls which drive transistors receive “image data” for each OLED. *Id.* at 1:36-38. Thus, the “signal lines” are differentiated from the other conductive lines on conventional OLED panels. *Id.*; *see also id.* at 16:14-34, 17:19-40, 19:17-23, 19:31-46, 30:30-51, Figs. 2, 21.

Solas’s construction—a conductive line supplying signals of any kind—is overbroad and ignores that “signal lines” are distinguished in the claims and specification from “supply lines” and “scan lines” based on the signals they each carry. Solas’s construction would subsume all three types of conductive lines without differentiating them in any way, which cannot be correct. *CAE Screenplates*, 224 F.3d at 1317. In short, the proper construction of signal lines, and the only one that will help the jury understand what the inventors meant by “signal lines” in the context of the ’068 patent, is “conductive lines supplying a value corresponding to a luminance level.”

D. “feed interconnections” (claims 1, 10, 12, 13, 17)

Defendants’ Proposed Construction	Solas’s Proposed Construction
Conductive structures in a layer or layers different from the gates, sources, and drains that provide connections to a source that supplies voltage and/or current.	Conductive structures in a layer or layers that provide connections to a source that supplies voltage and/or current.

“Feed interconnections” refers to conductive structures “formed on” or “connected to” the

supply lines as noted above. The parties agree that these structures are “in a layer or layers” of the circuit. Defendants’ construction clarifies that the “feed interconnections” are formed in a layer or layers that are different from the layer of the gate, source, and drain of the driving transistors.

The purpose of the “feed interconnections” is to avoid the “voltage drop” and “delay” problems caused when “interconnections such as a power supply line” are patterned *together with* the layers in which the gates, sources and drains are formed. *Supra* at Sections V.A, V.B; *see also* ’068 patent at 1:57-2:35; Holberg ¶¶ 120-126. So as the “Summary of the Invention” states, the “feed interconnections” are “formed *separately* for [sic: *from*] the drains, sources, and gates of the driving transistors.” *Id.* at 3:61-64; *see also id.* at 18:26-40; *Wireless Protocol Innovations, Inc. v. TCT Mobile, Inc.*, 771 F. App’x 1012, 1018 (Fed. Cir. 2019) (explaining statements in the “Summary of the Invention” section are meant to describe the overall invention and can “make clear” requirements of the claim). Defendants’ construction reflects this requirement.

Because “feed interconnections” does not have a “plain or established meaning,” it cannot be construed more broadly than the specification’s disclosure. Holberg ¶ 119; *Vehicle IP, LLC v. Celco P’ship*, 757 F. App’x 954, 958 (Fed. Cir. 2019) (“[B]ecause the term lacks a plain or established meaning, the court should not construe ‘dispatch’ more broadly than the specification’s disclosure.”). The specification teaches that in every embodiment, the “feed interconnections” are “formed from a conductive layer different from the gates, sources and drains of thin-film transistors.” ’068 patent at 18:30-33; *see also id.* at 10:25-32, 26:61-66, Figs. 8, 25. It is “*for this reason*”—that the feed interconnections are formed in a different layer—that the “voltage drop by the feed interconnections 90 is small” and “the write current (pull-out current) can sufficiently be supplied without any delay.” ’068 patent at 18:32-39. This is essential, as the “*object of the present invention* [is] to satisfactorily drive a light-emitting element while *suppressing any voltage drop*

and signal delay.” *Id.* at 2:38-41; *cf id.* at 18:26-29 (describing layers with the “gate or the source/drain” have a resistance that is “too high”), 2:5-35 (explaining that interconnects formed in TFT layers cause “voltage drop” and “delay” problems); Holberg ¶¶ 121-126. Defendants’ construction should therefore be adopted because “the very character of the invention” requires that the “feed interconnections” be formed in a layer different from the gates, sources and drains. *Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1370 (Fed. Cir. 2003).

Defendants’ construction is also compelled by the applicant’s statements in the prosecution history. In response to a restriction requirement, the applicants elected to proceed with claims drawn to a single species of their claimed inventions, an embodiment “wherein the feed interconnections are formed from a conductive layer *different from the gate, source and drain* of the TFTs of the pixel electrode.” Ex. 20 at 2. The law does not permit Solas to recapture in court today claim scope that the applicants surrendered years ago before the Patent Office when they applied for the patent. *See Uship Intellectual Properties, LLC v. United States*, 714 F.3d 1311, 1315 (Fed. Cir. 2013). “Feed interconnections” thus should be construed to mean “conductive structures in a layer or layers different from the gates, sources, and drains that provide connections to a source that supplies voltage and/or current.”

VI. CONCLUSION

For the reasons explained above, Defendants respectfully request that the Court issue an order adopting their proposed constructions of the disputed claim terms.

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Respectfully Submitted

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